AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for determining critical timing path sensitivities of macros in a semiconductor device, comprising:

accessing a first file including information indicative of at least one test operation;

configuring a timing parameter of a particular macro in the semiconductor device based on the information included in the first file;

determining a first maximum operating frequency of the semiconductor device configured in accordance with the timing parameter;

modifying a second file including information indicative of a configuration of the semiconductor device;

changing the timing parameter of the particular macro;

determining a second maximum operating frequency of the semiconductor device configured in accordance with the changed timing parameter and the second file; and

determining a contribution of the selected macro to a critical timing path of the semiconductor device based on the first and second maximum operating frequencies.

2. (Original) The method of claim 1, wherein configuring the timing parameter further comprises configuring a self-timed pulse control (STPC) parameter of the selected macro.

3. (Original) The method of claim 2, wherein changing the timing parameter further comprises decreasing the STPC parameter.

4. (Original) The method of claim 3, wherein determining the contribution of the selected macro to the critical timing path of the semiconductor device further comprises determining that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being greater than the first maximum operating frequency.

5. (Original) The method of claim 2, wherein changing the timing parameter further comprises increasing the STPC parameter.

6. (Original) The method of claim 5, wherein determining the contribution of the selected macro to the critical timing path of the semiconductor device further comprises determining that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being less than the first maximum operating frequency.

7. (Original) The method of claim 1, wherein determining the contribution of the selected macro to the critical timing path of the semiconductor device further comprises determining that the selected macro has a limited effect on the critical timing path in response to the second maximum operating frequency being substantially the same as the first maximum operating frequency.

8. (Original) The method of claim 1, further comprising changing a default STPC setting of the selected macro based on the first and second maximum operating frequencies.

9. (Currently Amended) A system for testing a semiconductor device including a plurality of macros, comprising:

a tester configured ~~adapted~~ to access a first file including information indicative of at least one test operation, configure a timing parameter of a particular macro in the semiconductor device based on the information in the first file, determine a first maximum operating frequency of the semiconductor device configured in accordance with the timing parameter, modify a second file including information indicative of a configuration of the semiconductor device, change the timing parameter of the particular macro, and determine a second maximum operating frequency of the semiconductor device configured in accordance with the changed timing parameter and the second file; and

a controller configured ~~adapted~~ to receive the first and second maximum operating frequencies and determine a contribution of the selected macro to a critical timing path of the semiconductor device based on the first and second maximum operating frequencies.

10. (Original) The system of claim 9, wherein the timing parameter further comprises a self-timed pulse control (STPC) parameter of the selected macro.

11. (Original) The system of claim 10, wherein the tester is adapted to decrease the STPC parameter.

12. (Original) The system of claim 11, wherein the controller is adapted to indicate that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being greater than the first maximum operating frequency.

13. (Original) The system of claim 10, wherein the tester is adapted to increase the STPC parameter.

14. (Original) The system of claim 13, wherein the controller is adapted to indicate that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being less than the first maximum operating frequency.

15. (Original) The system of claim 9, wherein the controller is adapted to indicate that the selected macro has a reduced effect on the critical timing path in response to the second maximum operating frequency being substantially the same as the first maximum operating frequency.

16. (Currently Amended) A system for determining critical timing path sensitivities of macros in a semiconductor device, comprising:

means for accessing a first file including information indicative of at least one test operation;

means for configuring a timing parameter of a particular macro in the semiconductor device based on the information included in the first file;

means for determining a first maximum operating frequency of the semiconductor device configured in accordance with the timing parameter;

means for modifying a second file including information indicative of a configuration of the semiconductor device

means for changing the timing parameter of the particular macro;

means for determining a second maximum operating frequency of the semiconductor device configured in accordance with the changed timing parameter and the second file; and

means for determining a contribution of the selected macro to a critical timing path of the semiconductor device based on the first and second maximum operating frequencies.

17. (New) The method of claim 1, wherein modifying the second file comprises modifying the second file to modify information indicative of a JTAG mode of the semiconductor device.

18. (New) The method of claim 17, further comprising placing the semiconductor device into JTAG mode based on the information indicative of the JTAG mode.

19. (New) The method of claim 18, wherein placing the semiconductor device into JTAG mode comprises providing the information indicative of the JTAG mode to a JTAG register in the semiconductor device.